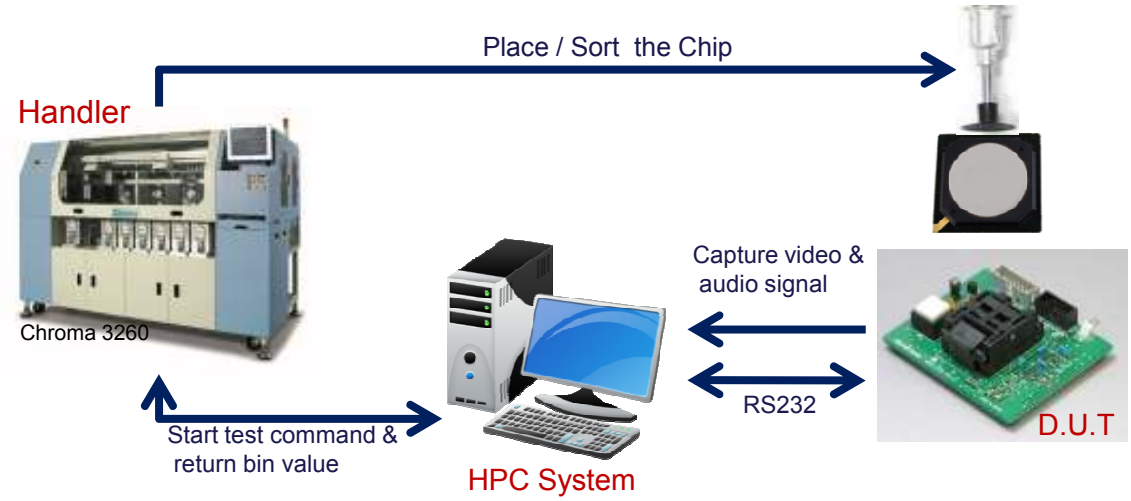
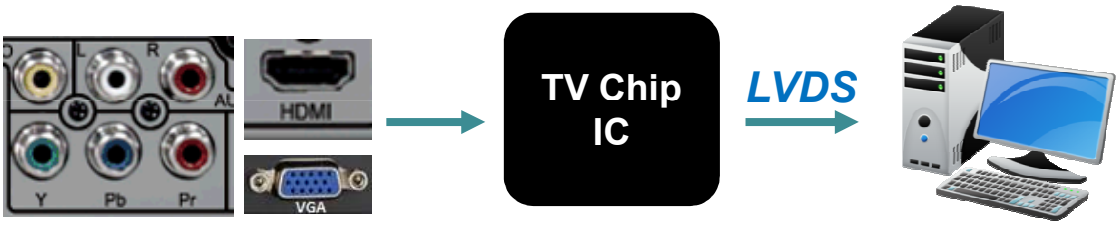
System Level Tester

LVDS Testing System

SLT Testing Procedure



HPC MTS-LVDS System



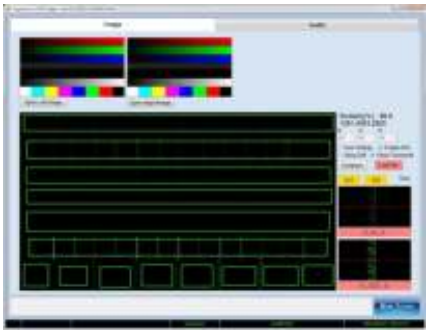
Data Source

MTS-LVDS

- ***Sort out the fail Chip***
- ***Friendly HMI***
- ***Directly to show what we capture***
- ***Tool Kit: for R/D to analyze the pixel difference***

● Main HMI

● Tool Kit



Specification	
Input Port	Dual LVDS Quad LVDS for 3D/120HZ (Option)
Resolution	1080P@60 1080P@120 (Option)
Pixel Color Depth	8 / 10 bit
Pixel Clock Rate	Dual LVDS(Single Port) 1920(2200)*1080(1125)*60Hz=148.5MHz max Quad LVDS(Dual Port) (Option) 1920(2200)*1080(1125)*120Hz=270MHz max
Support Data Format	VESA / JEIDA
Audio Input	Line-In(Stereo)
Serial Port	RS232 with Handler x 1 RS232 with Test Board x 2

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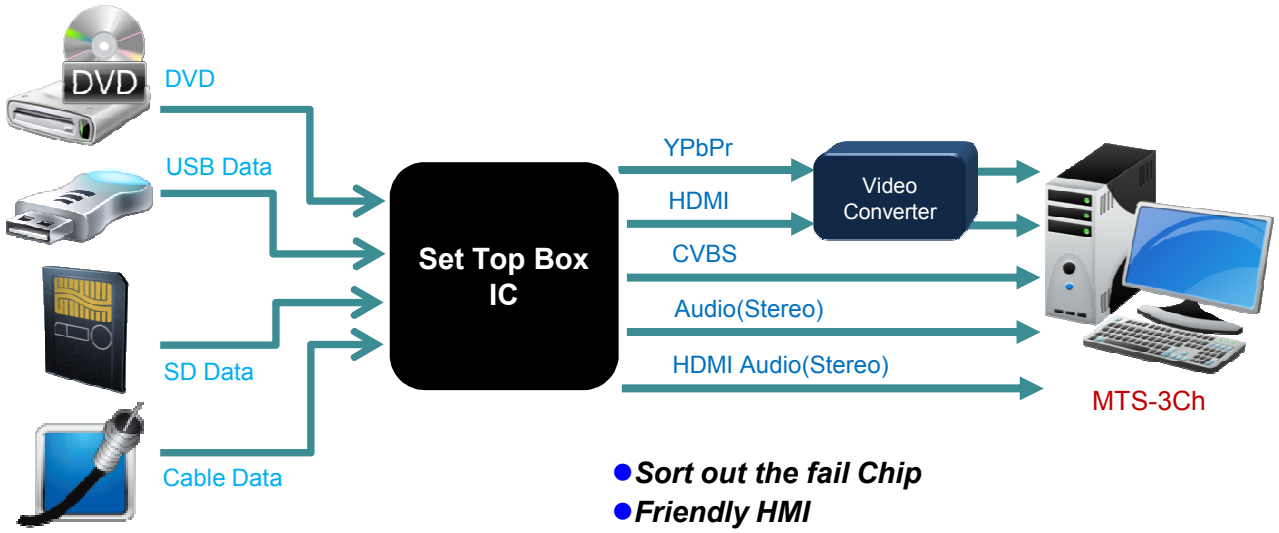
System Level Tester

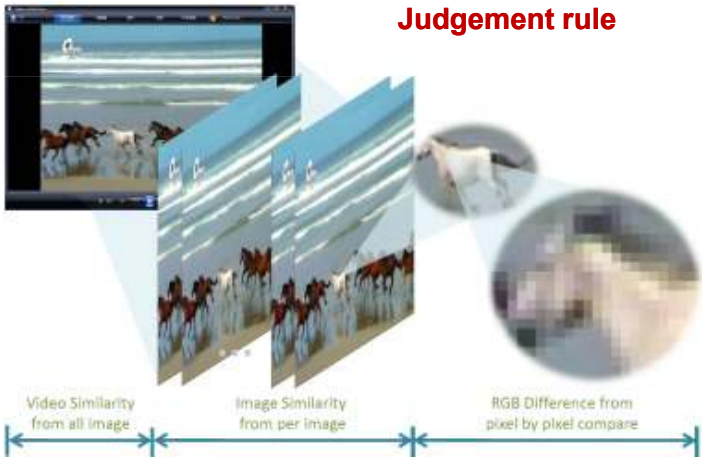
Multi-Channel AIV Testing System

HPC MTS-3Ch System



- ***Sort out the fail Chip***
- ***Friendly HMI***
- ***Capture Video & Audio Synchronously***

Judgement rule



- Main HMI

- Recipe Setting

Specification	
Video Signal	CVBS, YPbPr to CVBS, HDMI to CVBS
Video Format	NTSC, PAL
Resolution	NTSC: 640x480 (Max) PAL: 720x576 (Max)
Frame Rate	NTSC: 29.97 Frame / sec PAL: 25 Frame / sec
Audio Input	Line-In (Stereo)
Input Port	CVBS port x 3 Line-In port x 2

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